Fig. 1

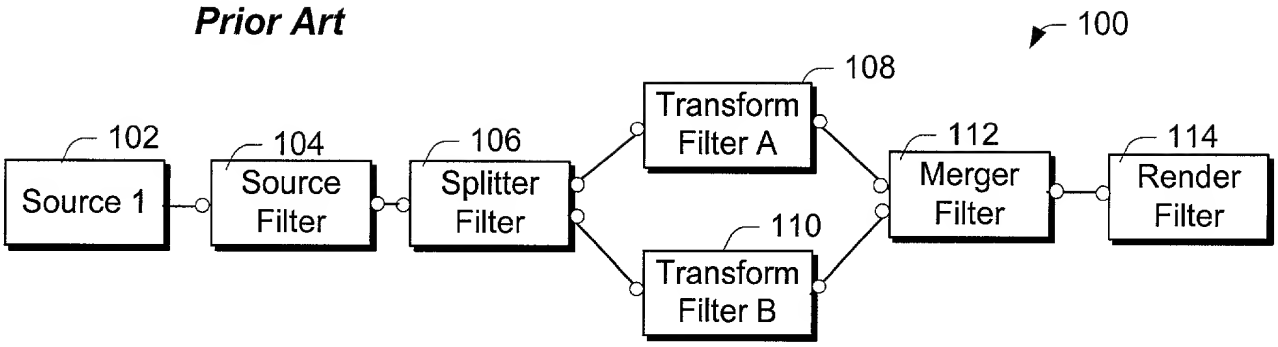
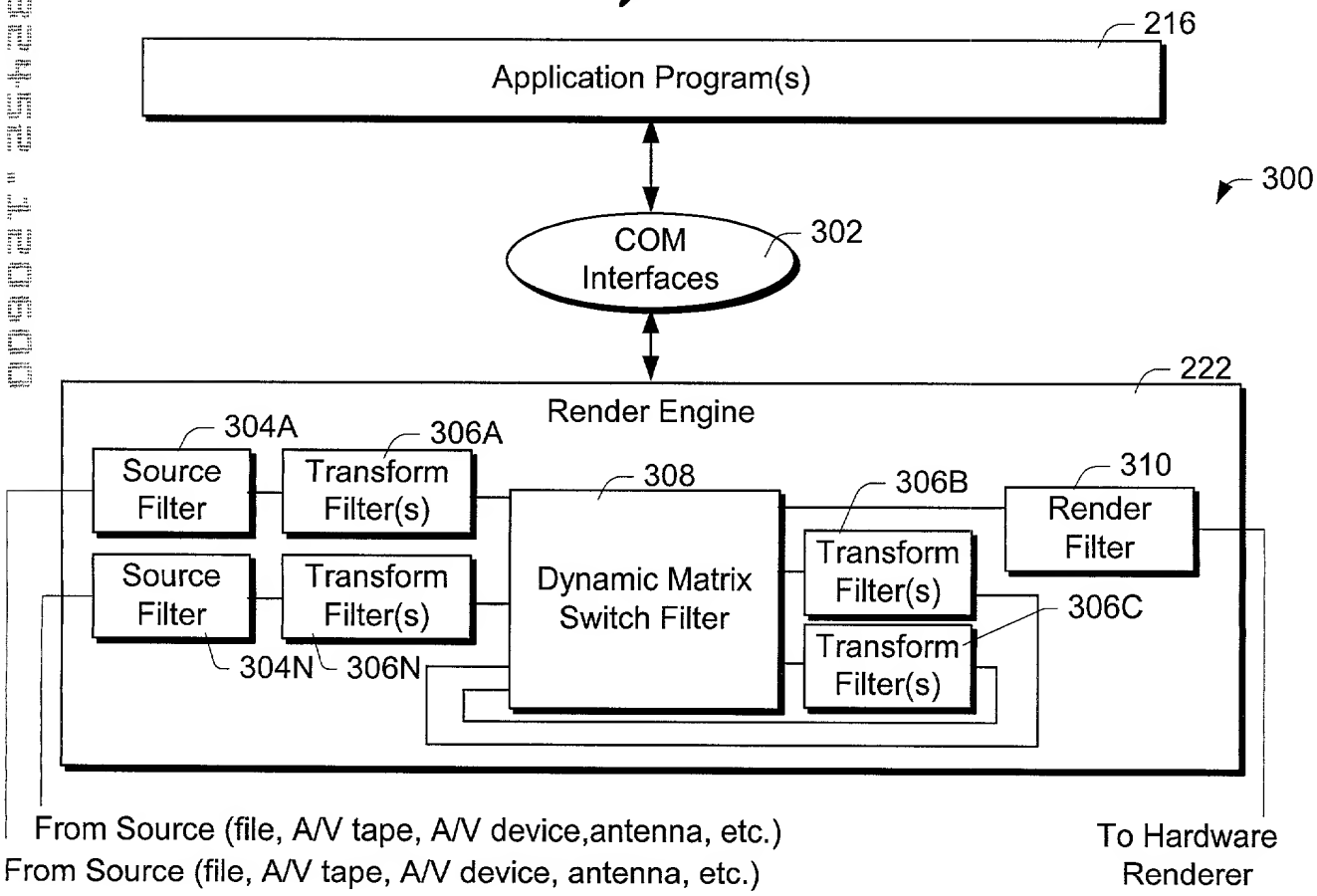

Prior Art
100
102
Source 1
104
Source Filter
106
Splitter Filter
108
Transform Filter A
110
Transform Filter B
112
Merger Filter
114
Render Filter

Fig. 3


216
Application Program(s)
300
COM Interfaces
302
222
Render Engine
304A
Source Filter
306A
Transform Filter(s)
Source Filter
Transform Filter(s)
304N
306N
308
Dynamic Matrix Switch Filter
306B
Transform Filter(s)
Transform Filter(s)
306C
310
Render Filter
From Source (file, A/V tape, A/V device,antenna, etc.)
From Source (file, A/V tape, A/V device, antenna, etc.)
To Hardware Renderer

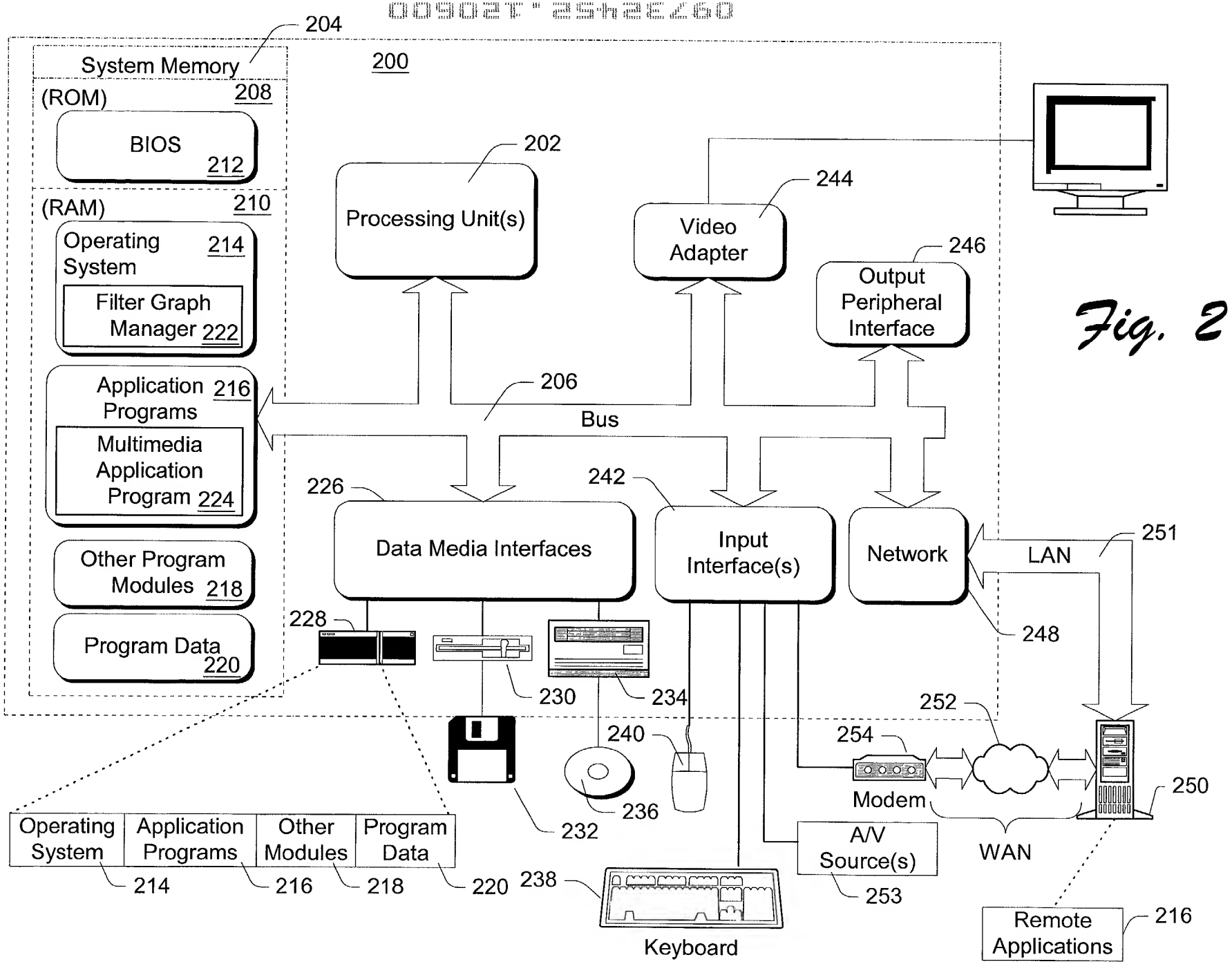


Fig. 2

Fig. 4

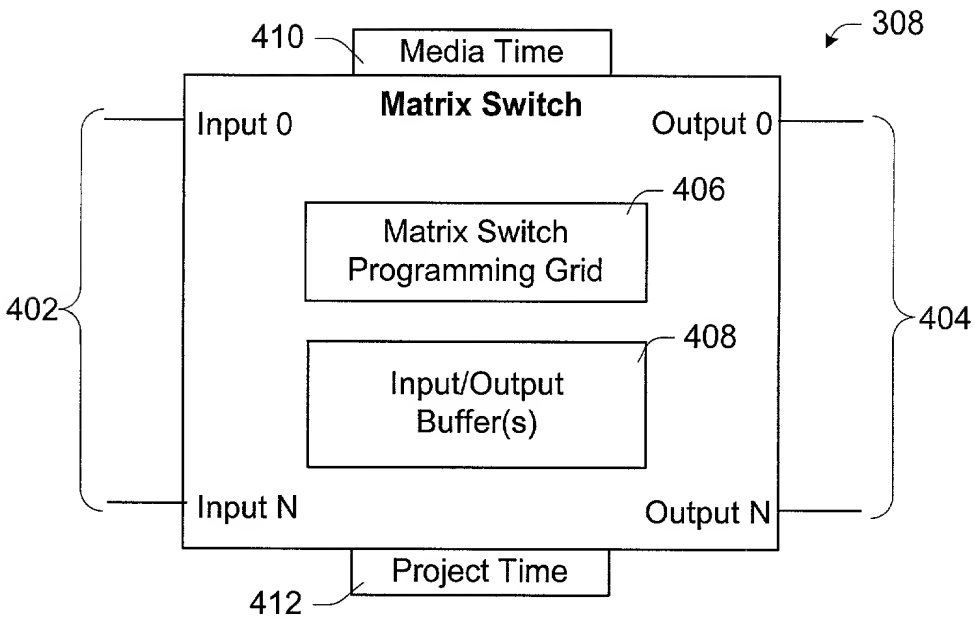
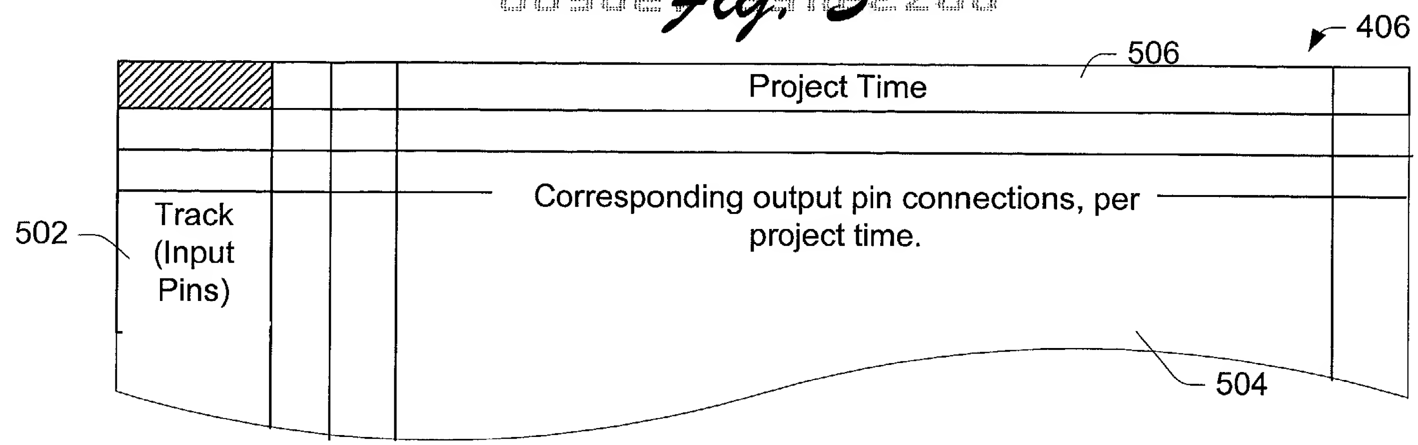
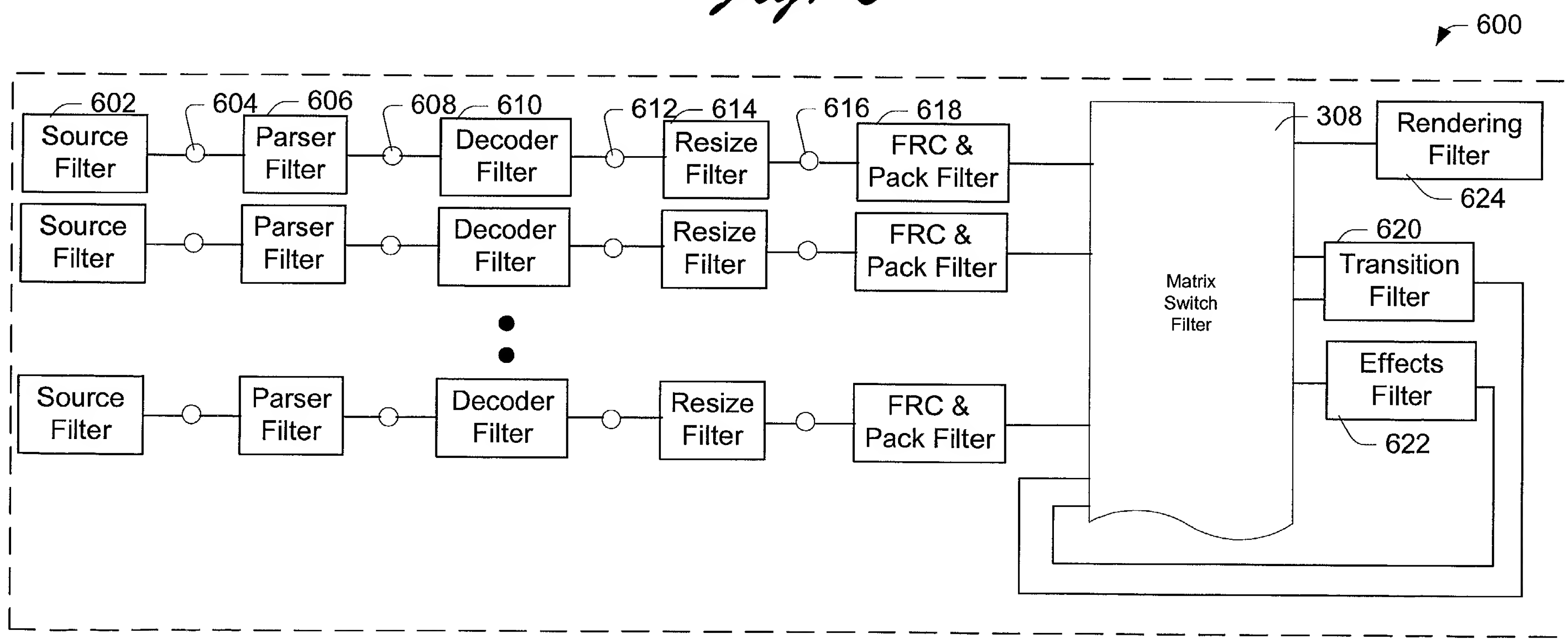

410
Media Time
308
Matrix Switch
Input 0
Output 0
406
Matrix Switch
Programming Grid
402
404
408
Input/Output
Buffer(s)
Input N
Output N
Project Time
412

Fig. 5



406
506
Project Time
502
Track (Input Pins)
Corresponding output pin connections, per project time.
504

Fig. 6



600
602
Source Filter
604
606
Parser Filter
608
610
Decoder Filter
612
614
Resize Filter
616
618
FRC & Pack Filter
308
Matrix Switch Filter
Rendering Filter
624
620
Transition Filter
Effects Filter
622

Fig. 7

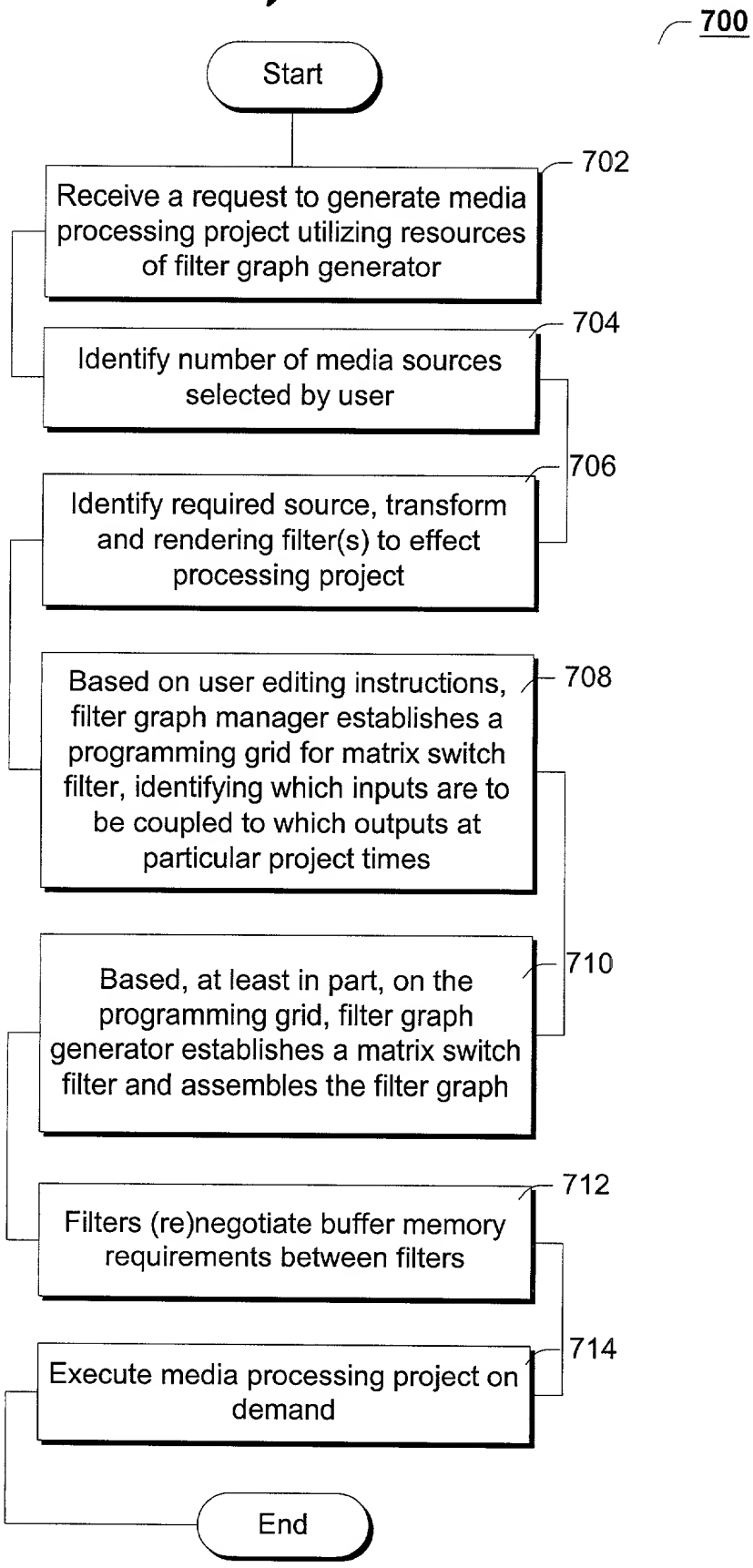
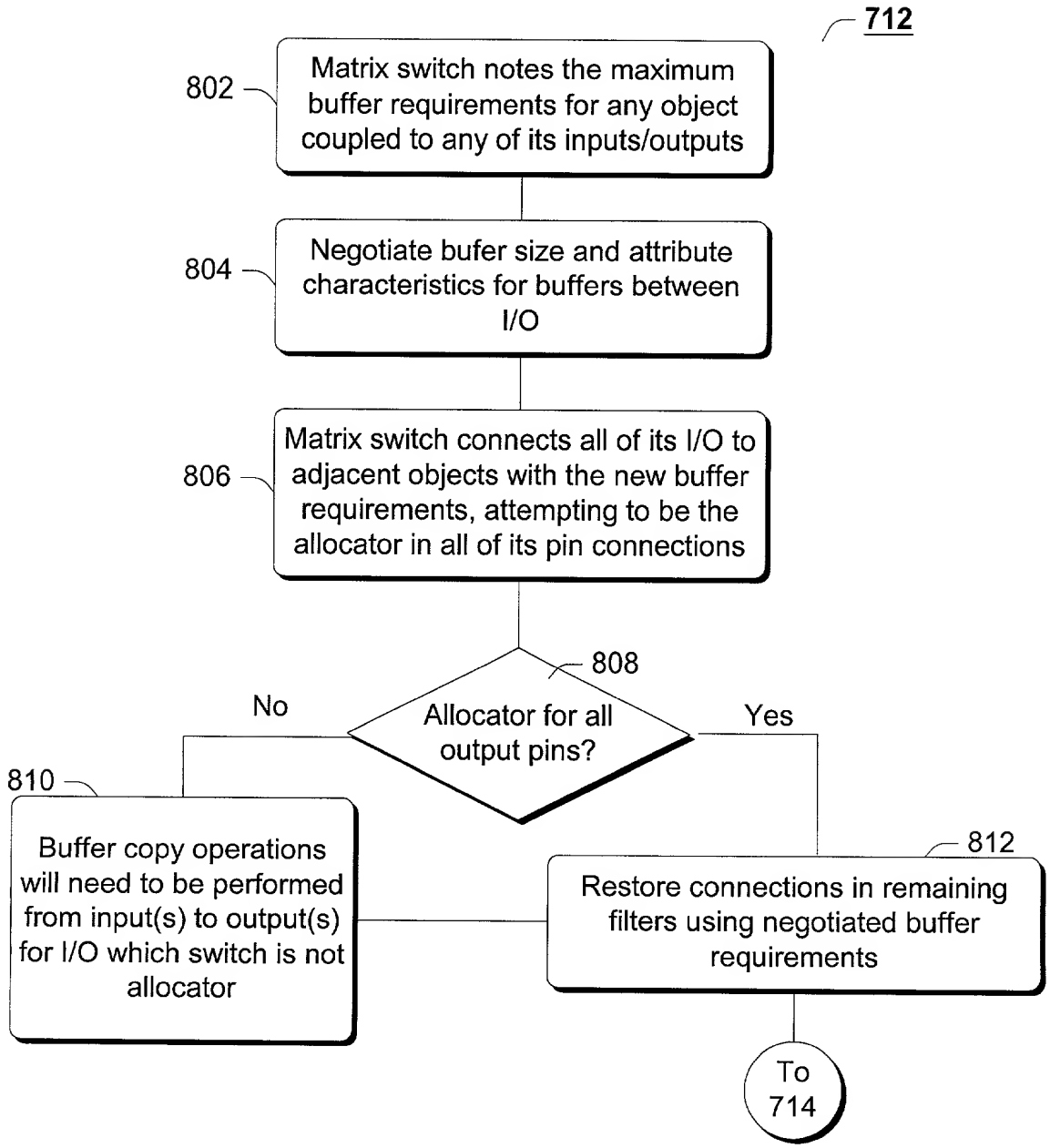


Fig. 8


712
802
Matrix switch notes the maximum buffer requirements for any object coupled to any of its inputs/outputs
804
Negotiate bufer size and attribute characteristics for buffers between I/O
806
Matrix switch connects all of its I/O to adjacent objects with the new buffer requirements, attempting to be the allocator in all of its pin connections
808
Allocator for all output pins?
No
Yes
810
Buffer copy operations will need to be performed from input(s) to output(s) for I/O which switch is not allocator
812
Restore connections in remaining filters using negotiated buffer requirements
To 714

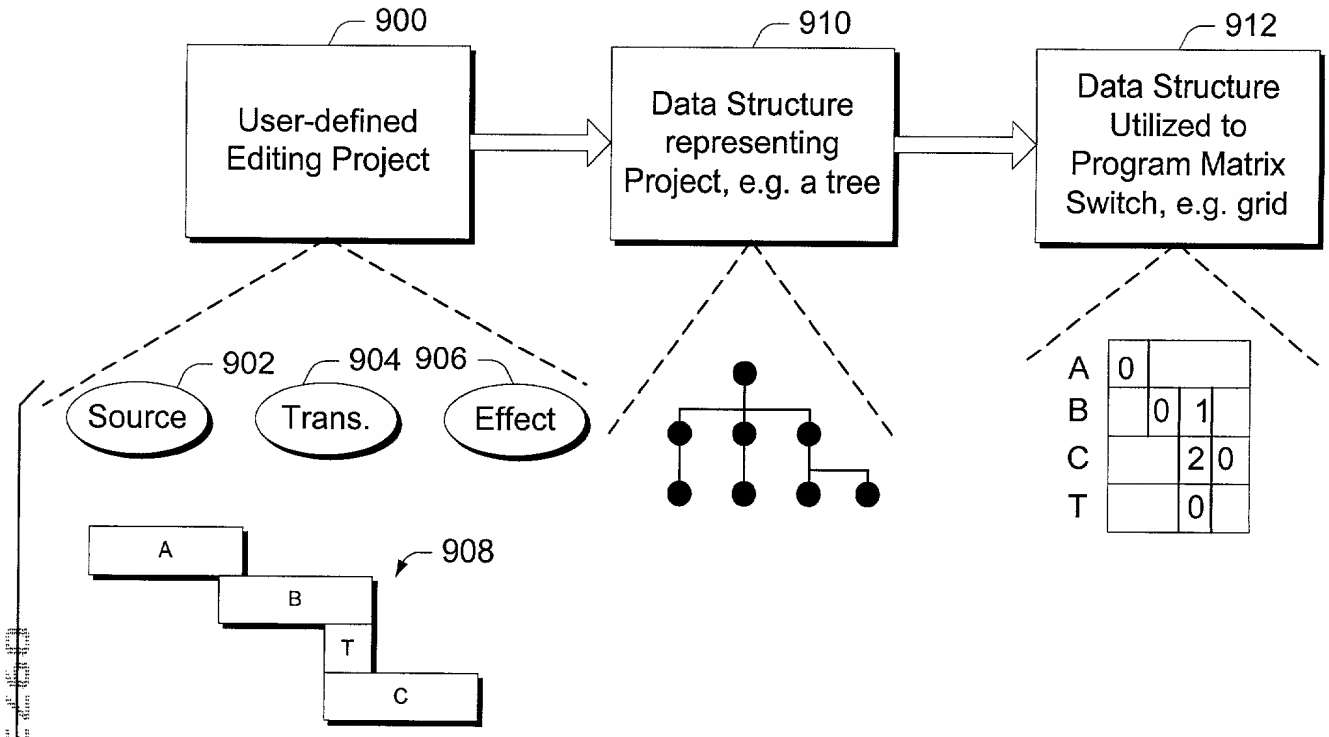

900
User-defined Editing Project
910
Data Structure representing Project, e.g. a tree
912
Data Structure Utilized to Program Matrix Switch, e.g. grid
902
904
906
Source
Trans.
Effect
A
B
C
T
0
0
1
2
0
0
A
B
T
C
908

Fig. 9

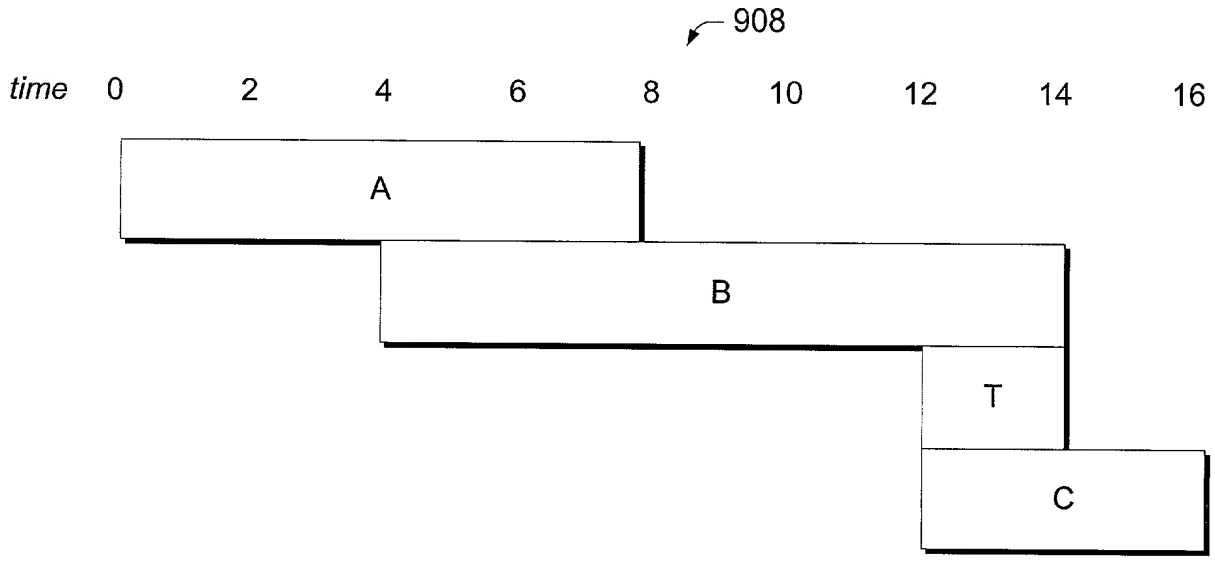

908
time
0
2
4
6
8
10
12
14
16
A
B
T
C

Fig. 10

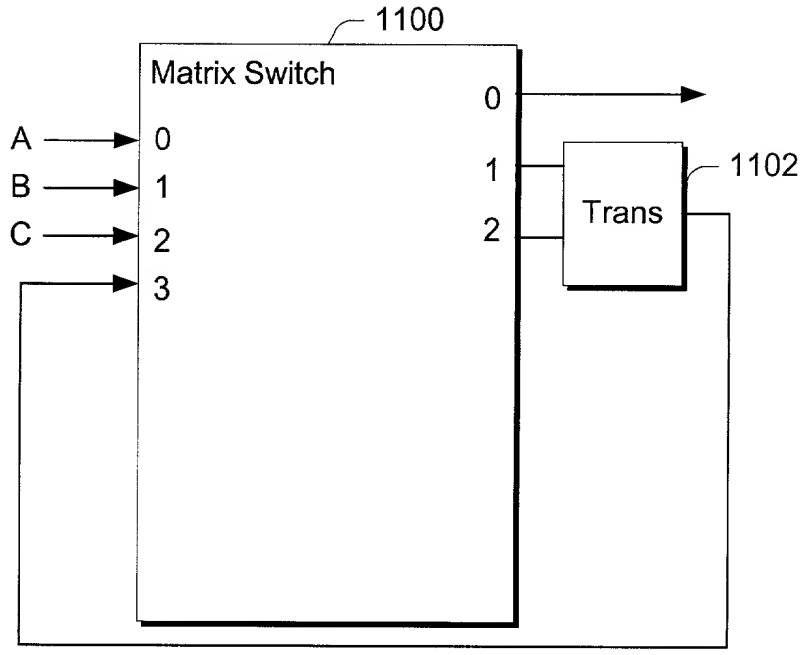

1100
Matrix Switch
A
B
C
0
1
2
3
0
1
2
Trans
1102

Fig. 11

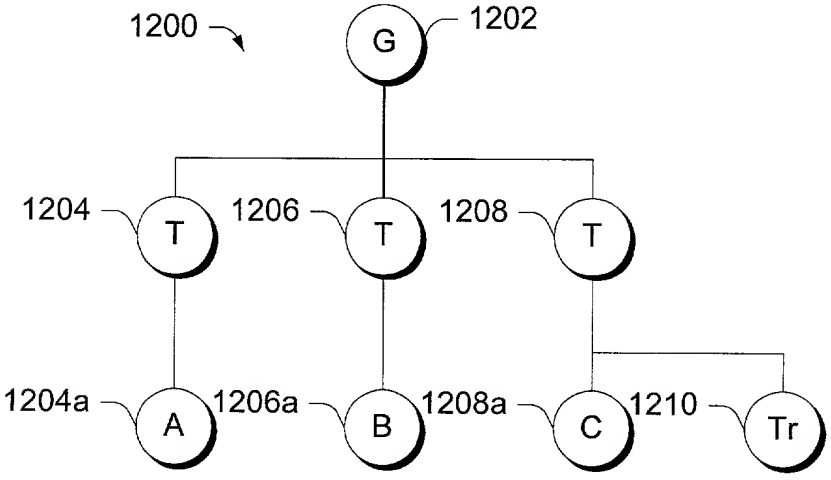

1200
G
1202
1204
T
1206
T
1208
T
1204a
A
1206a
B
1208a
C
1210
Tr

Fig. 12

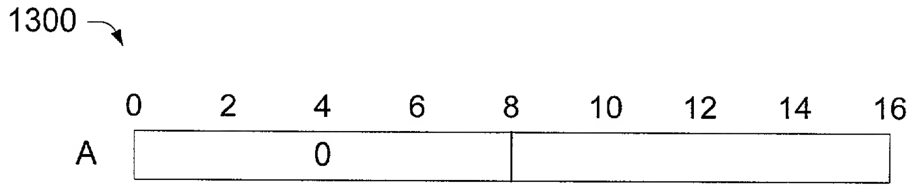


Fig. 13

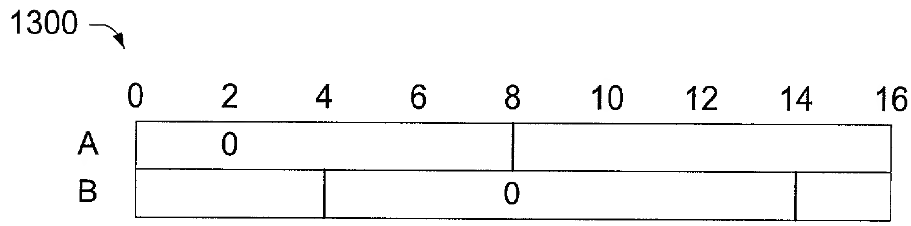


Fig. 14

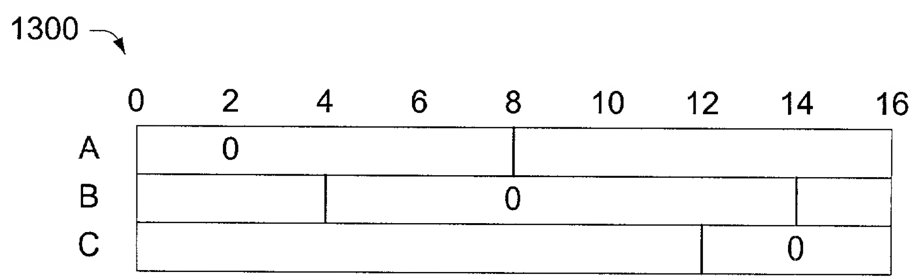


Fig. 15

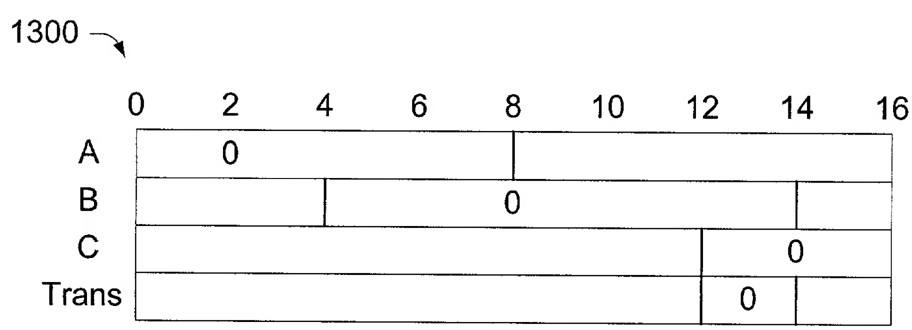


Fig. 16

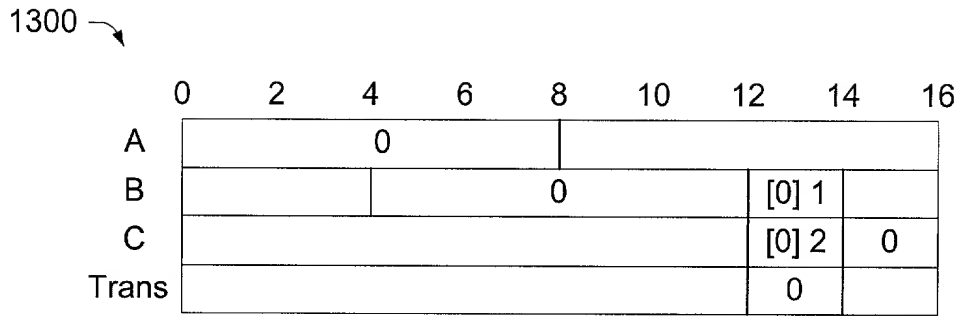


Fig. 17

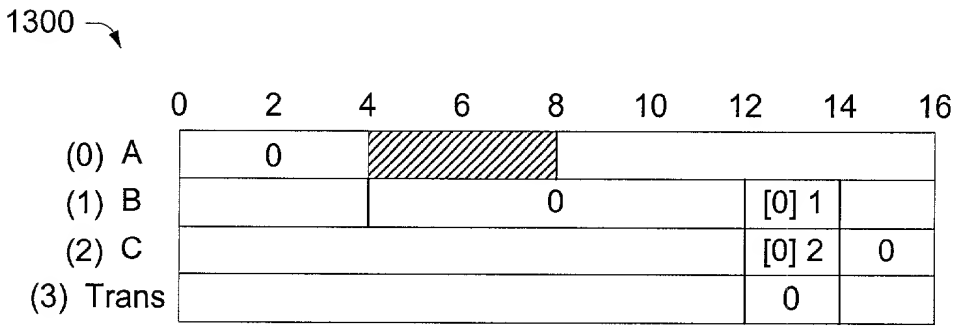


Fig. 18

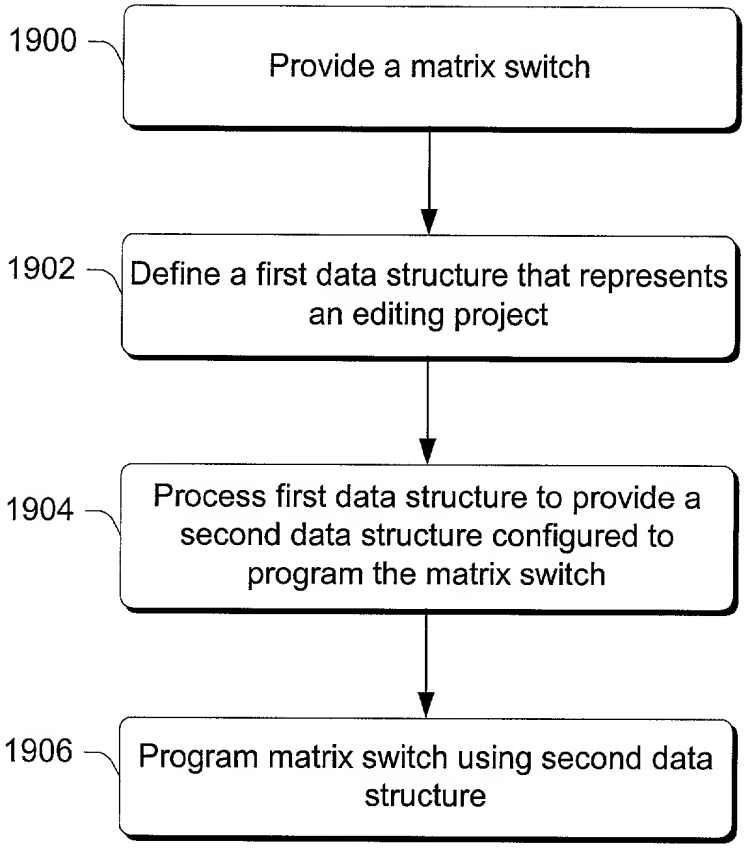

1900
Provide a matrix switch
1902
Define a first data structure that represents an editing project
1904
Process first data structure to provide a second data structure configured to program the matrix switch
1906
Program matrix switch using second data structure

Fig. 19

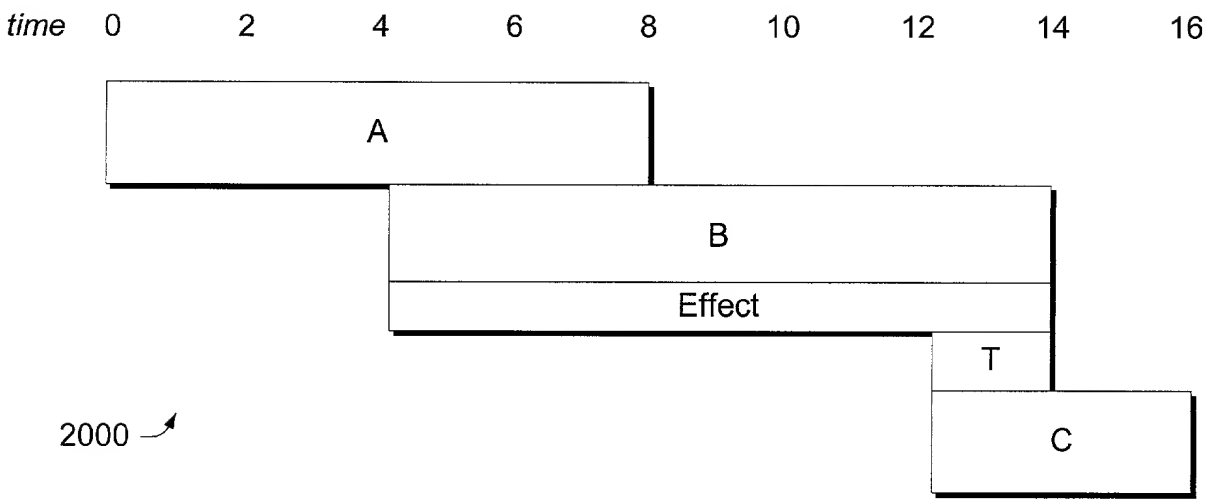


Fig. 20

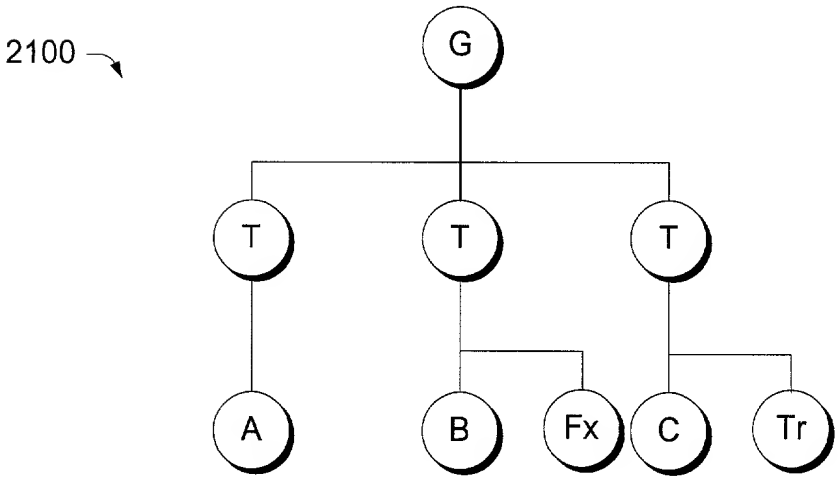


Fig. 21

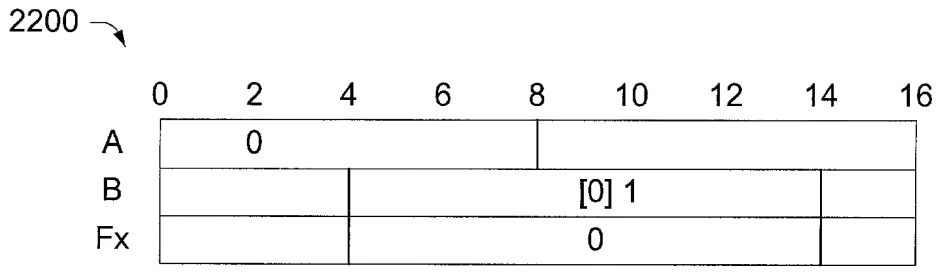


Fig. 22

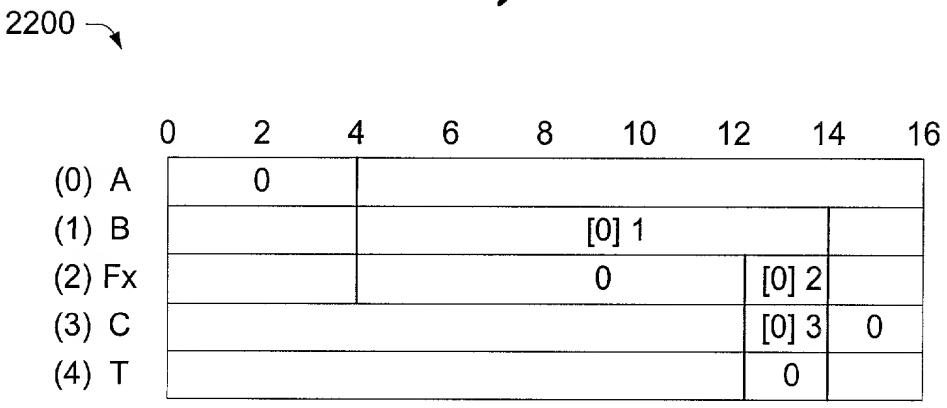


Fig. 23

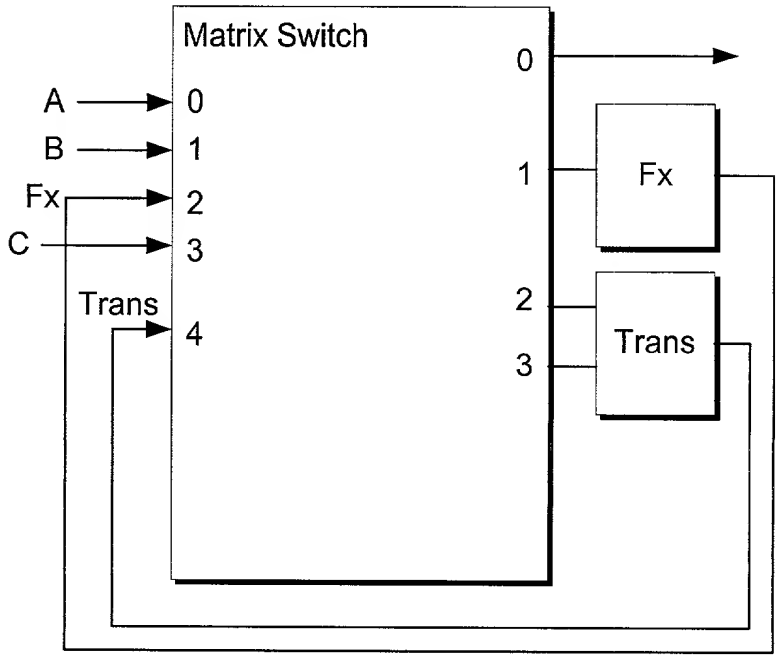


Fig. 24

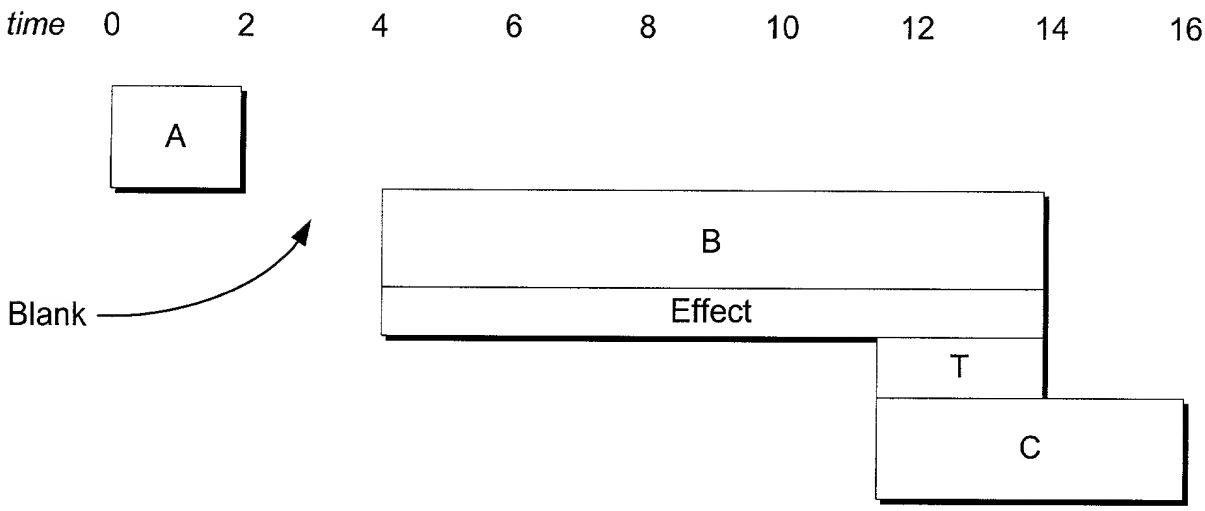


Fig. 25

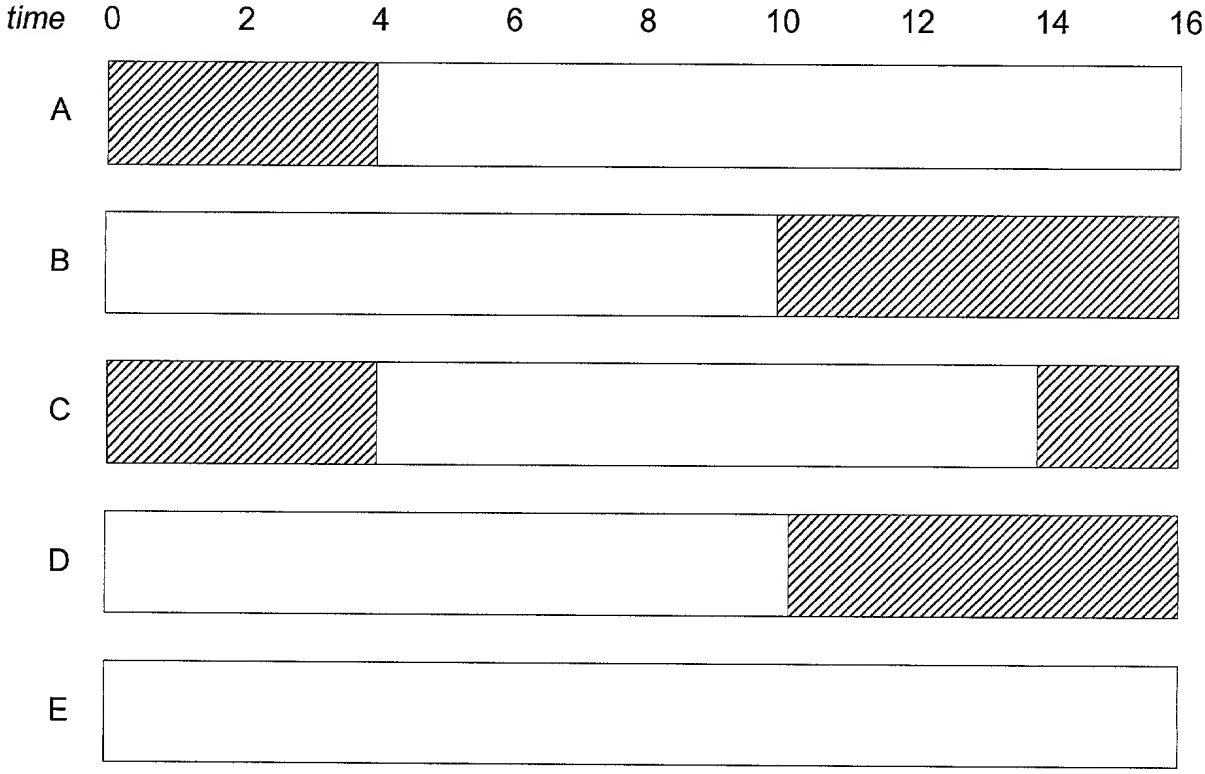


Fig. 26

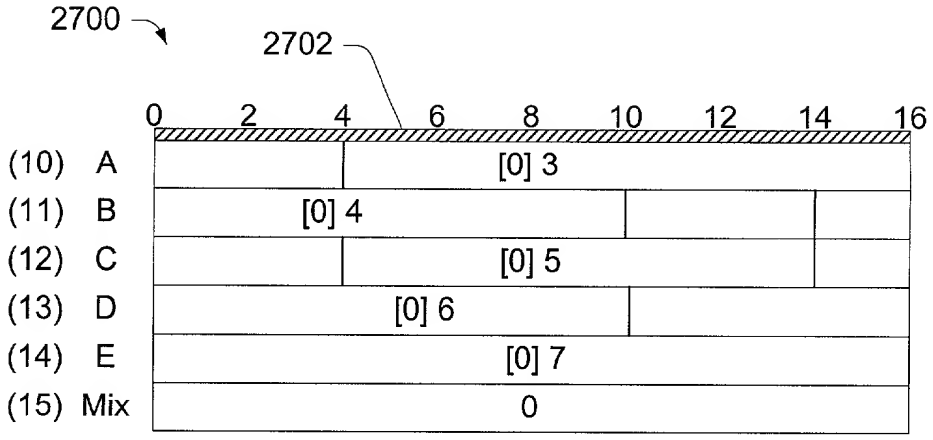

2700
2702
0
2
4
6
8
10
12
14
16
(10) A
(11) B
(12) C
(13) D
(14) E
(15) Mix
[0] 3
[0] 4
[0] 5
[0] 6
[0] 7
0

Fig. 27

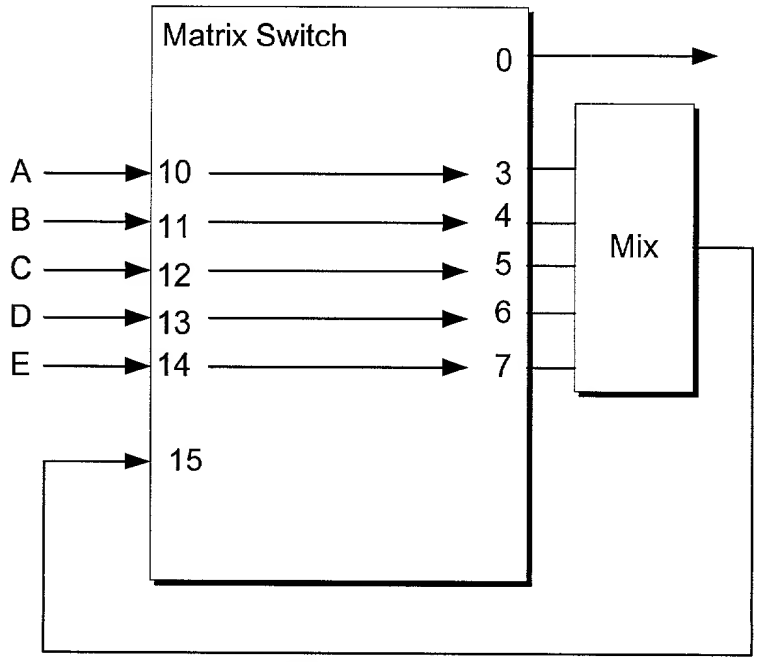

Matrix Switch
0
A
B
C
D
E
10
11
12
13
14
15
3
4
5
6
7
Mix

Fig. 28

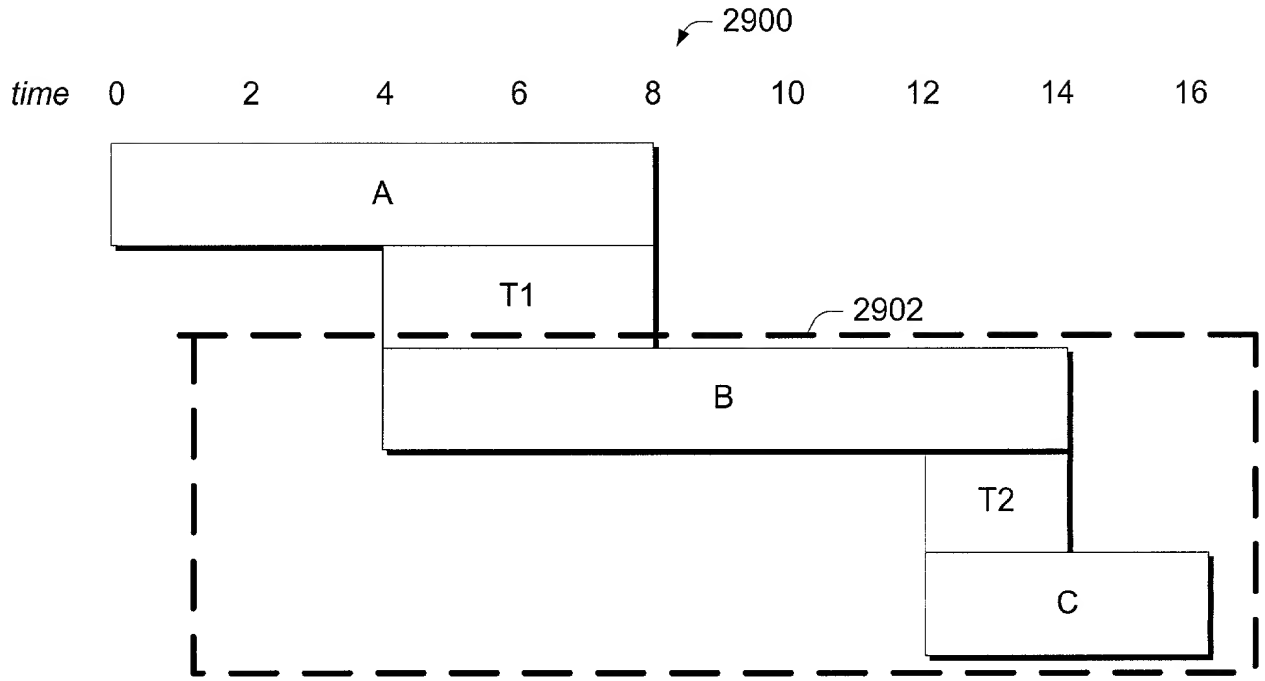

2900
time
0
2
4
6
8
10
12
14
16
A
T1
2902
B
T2
C

Fig. 29

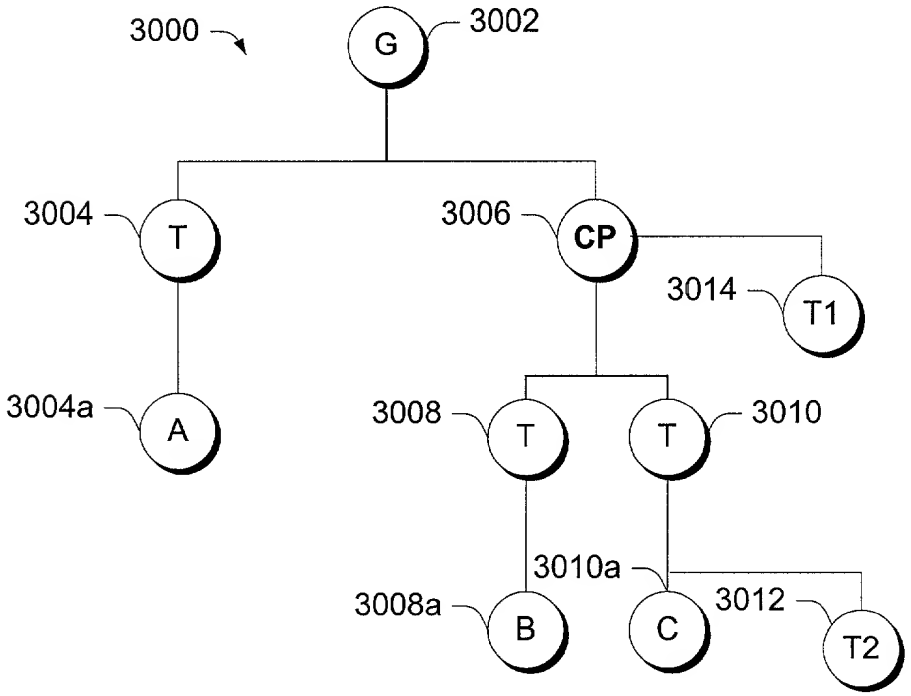

3000
G
3002
3004
T
3006
CP
3014
T1
3004a
A
3008
T
T
3010
3010a
3008a
B
C
3012
T2

Fig. 30

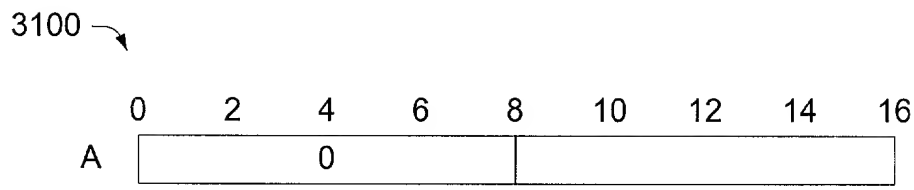


Fig. 31

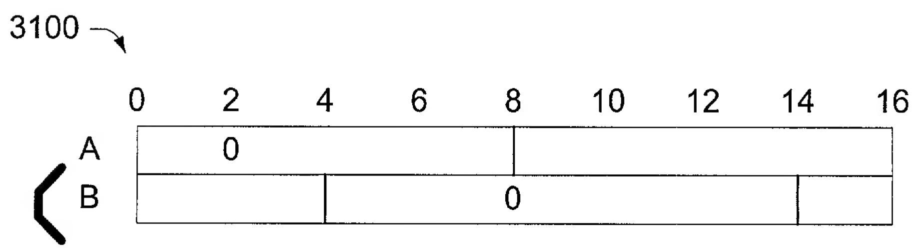


Fig. 32

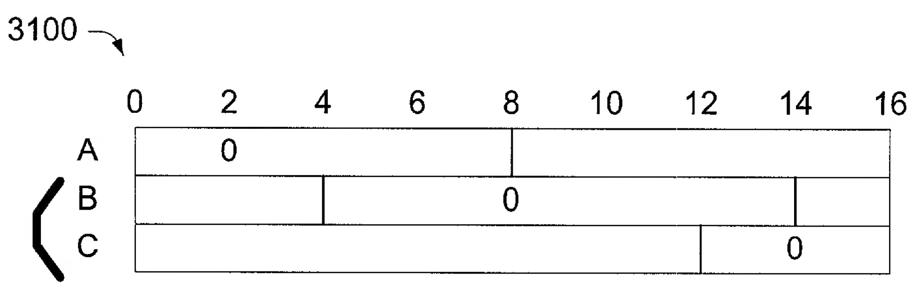


Fig. 33

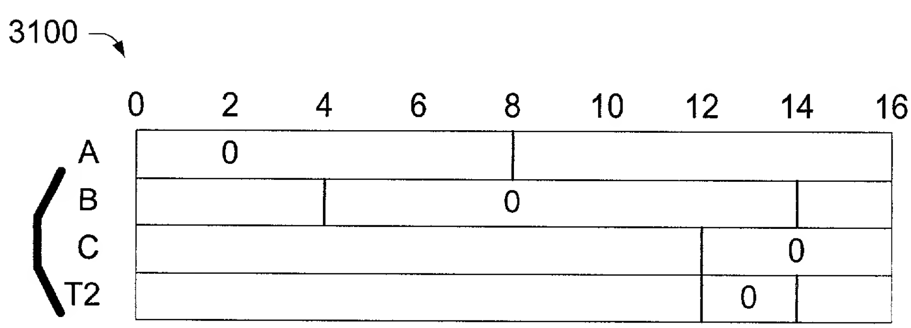


Fig. 34

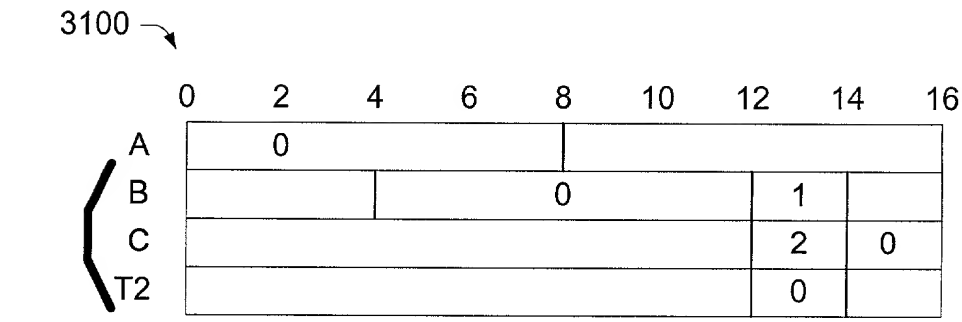


Fig. 35

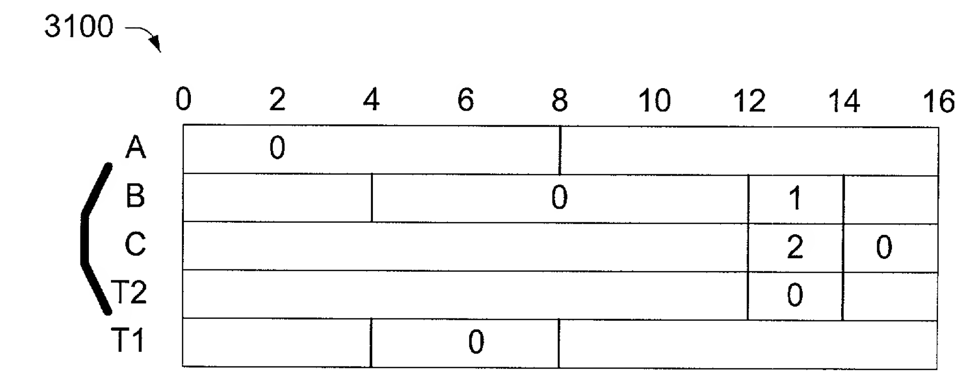


Fig. 36

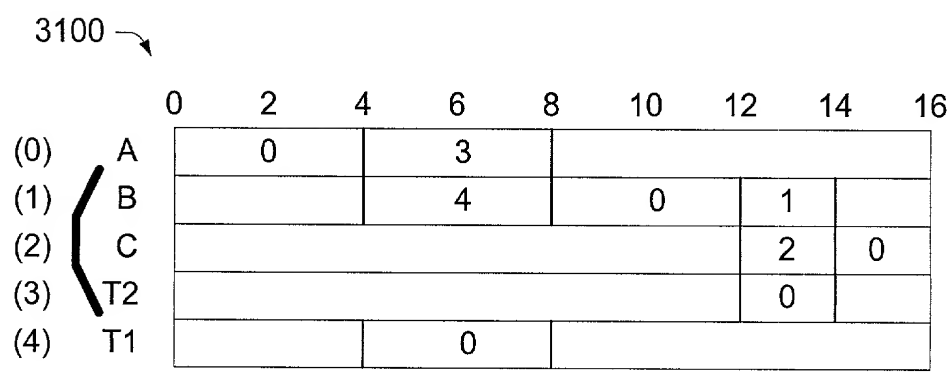


Fig. 37

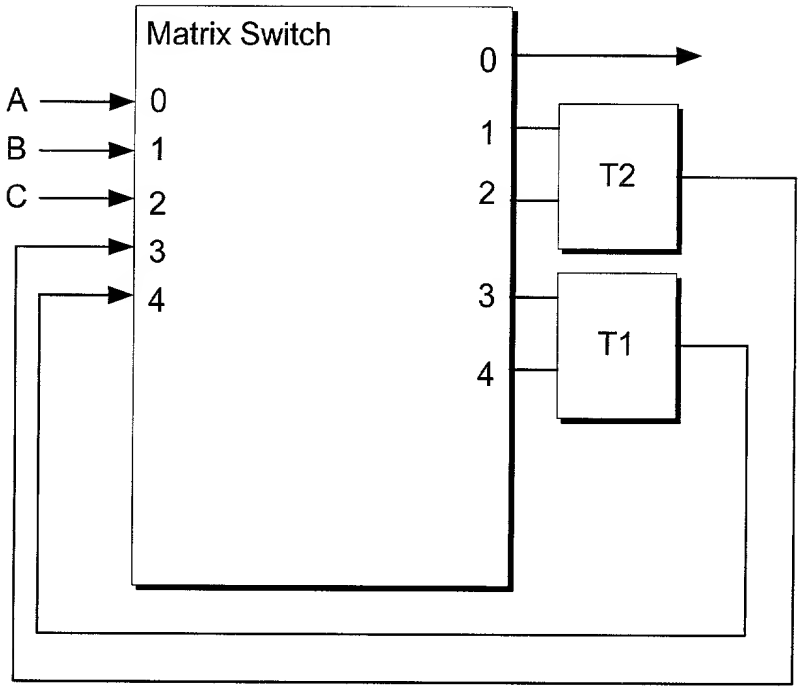


Fig. 38

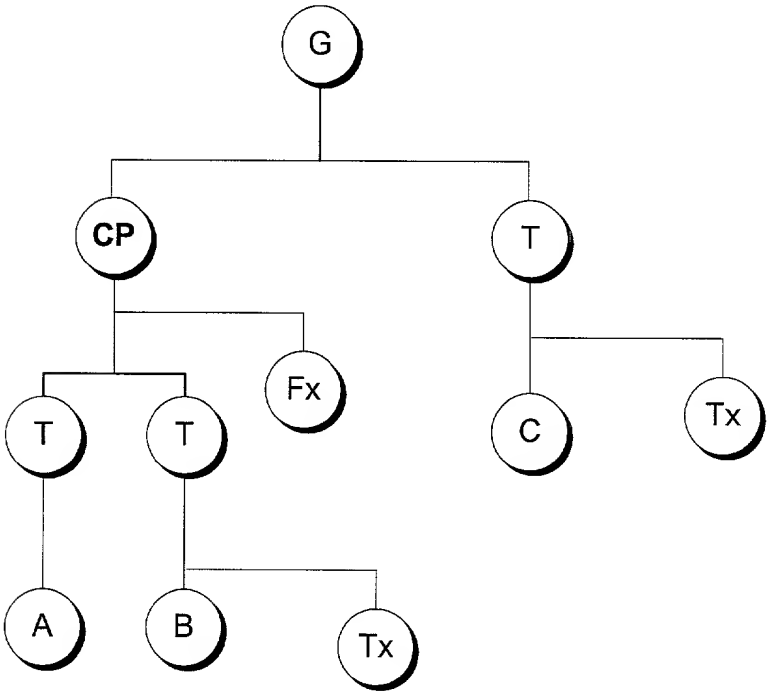


Fig. 38a

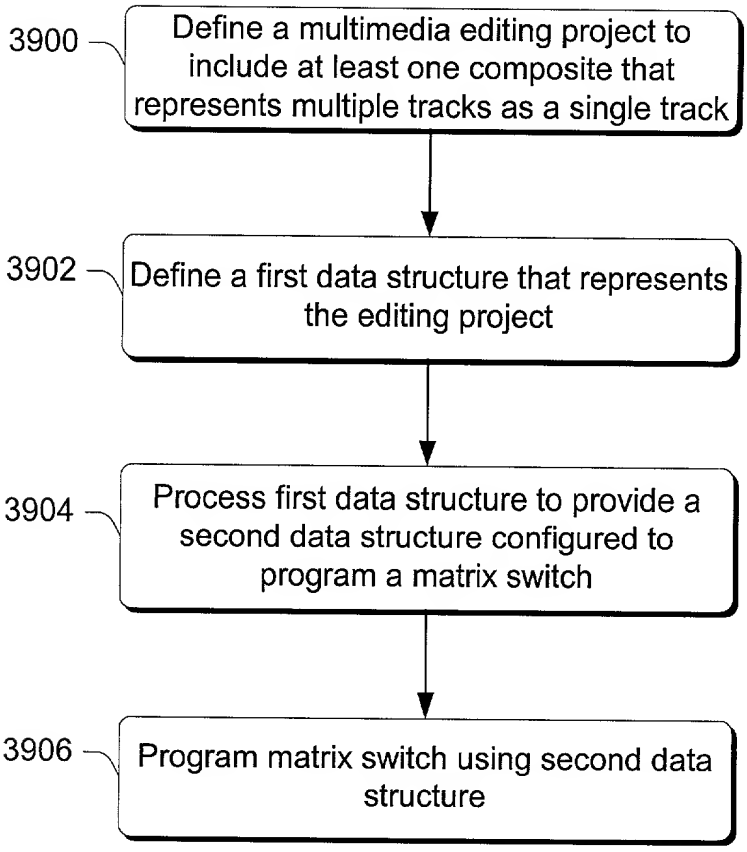


Fig. 39